

Press Release

Eindhoven, March 30, 2010

ASD Software Patent Awarded to Verum

Patent recognizes Verum's groundbreaking method for enabling software architects to profit from the science of Formal Methods without having expertise in mathematics

Verum Software Technologies (Waalre, Netherlands) announced that it received a European Patent on its Analytical Software Design (ASD) technologies during the company's annual ASD User Group event in Eindhoven. The patent (# EP1749264) recognizes, for the first time, an elegant method of applying Communicating Sequential Processes (CSP - a Formal Methods technique) algebras to develop defect free software architectures and software codes which are event driven and exhibit lots of concurrency. In the past, software architects were not able to enjoy the benefits of Formal Methods as they were deemed too difficult to learn, understand, and too expensive to apply and maintain for common code bases.

The ASD patent describes an integrated model based tool which allows software development experts to produce formal specifications and verified system designs that fully integrate into existing conventional software development processes. Fully integrated in this context means that there are continuous feedback loops into the software development process for handling errors extensions and modification arising in standard software development processes. A typical process is shown here in Figure 1, highlighting the functionality of ASD in such a process. The gap between the formal specifications and designs produced using ASD and the rest of the software development cycle is bridged for the first time. The consequence of this is that traditional errors made during requirements analysis, architecture specification and design, component specification and design are prevented from reaching the implementation, testing, and integration phases of software projects.

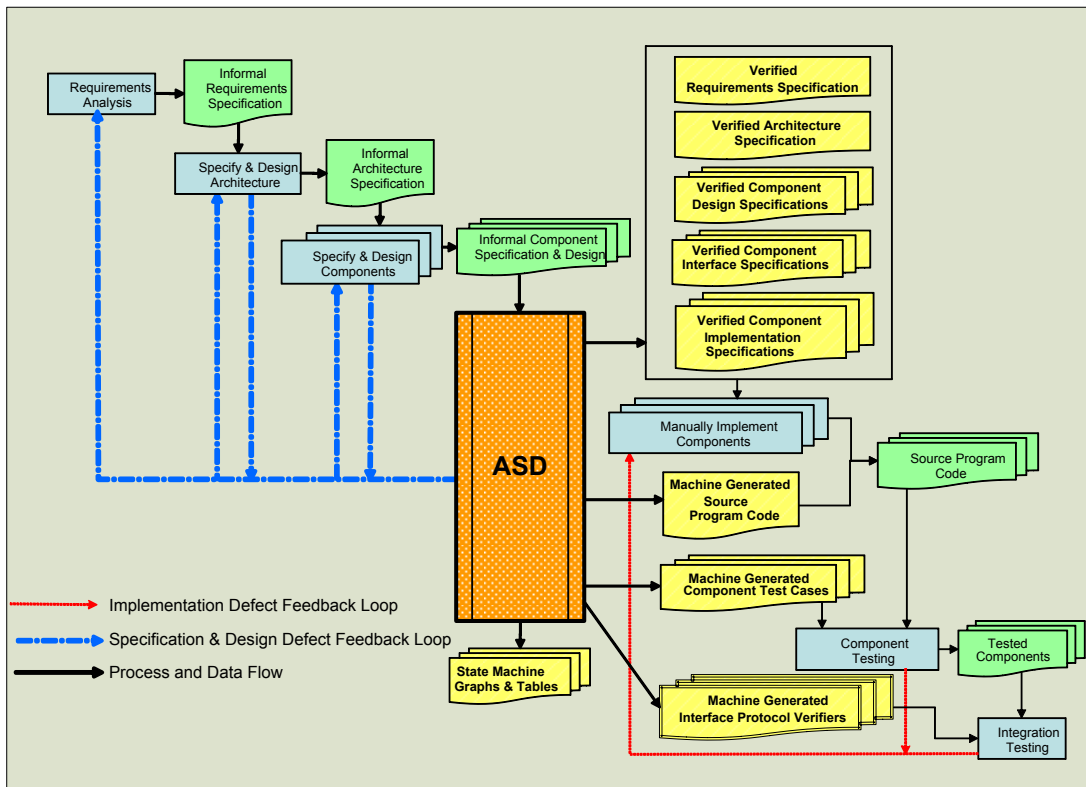


Figure 1 - The role of ASD in model based software development processes. The yellow boxes represent outputs from Verum's patented technology

Guy Broadfoot, the co-inventor of ASD, and Verum's C.T.O. said, "Hardware logic designers have long enjoyed the benefits of electronic design automation (EDA) tools enabling them to verify complex designs before implementation. ASD is a major step towards the goal of software design automation (SDA), being the first tool chain to make software design time verification a routine reality for software engineers. The patent grant is a very exciting milestone for Verum recognising as it does the unique contribution of Verum in this field."

The ASD patented technology is made available to users via an integrated desk top application called ASD:Suite. The application is shown in Figure 2. Users build proprietary models via a desktop client protecting their IP, and check these models using the patented ModelChecker technology which runs on Verum's servers. Once this step is complete, another patented component, the ASD CodeGenerator, automatically generates source codes in a variety of commonly used programming languages (C, C++, Java, C#) from the verified designs. This is a crucial part of the invention as it ensures that no human errors are introduced into the verified designs and it vastly speeds to process of generating production quality code.

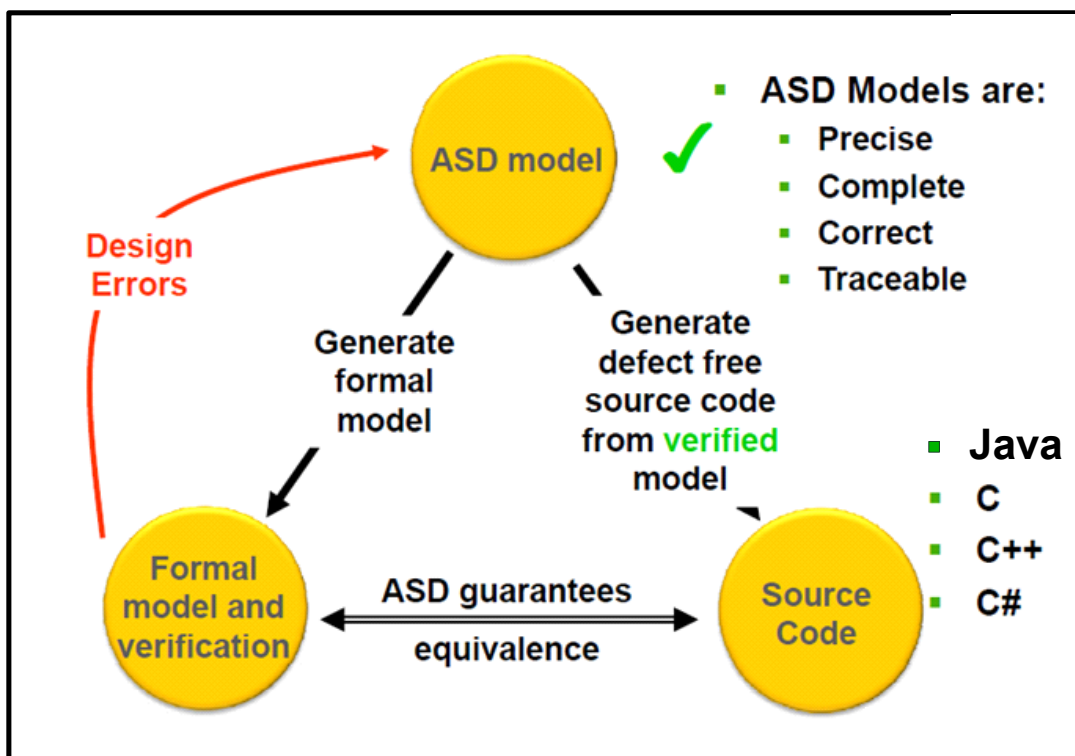


Figure 2 ASD:Suite Components

Thus far numerous customers such as Philips Medical Systems, Bosch, Logica, FEI, and others are using ASD in several countries around the world. Most projects involve generating tens or hundreds of thousands of lines of codes mathematically proven to be defect free

About Verum Software Technologies B.V.

Verum Software Technologies is a young software tools company focused on turning the art of software development into a fact based science. By adopting formal math based principals for embedded software development, embedded software manufacturers guarantee that such software codes are genuinely defect free in the 21st century. Verum employs a team made up of Formal Methods, Embedded Software Architects, and Embedded Software Tools experts to develop state of the art tools for achieving this goal. The company also provides consulting support to help propagate this paradigm shifting way of working in the software industries of the world. For more information see: www.verum.com

About Verum's ASD:Suite

Verum's ASD:Suite software design toolset eliminates all behavioural defects from complex software designs, dramatically cutting the cost of software development, testing and maintenance. ASD:Suite automatic code generation further reduces the cost of software development by 30% per delivered line of code. The key difference between Verum's ASD:Suite and tools that claim to improve productivity is Verum's Analytical Software Design formal verification technology; ASD allows the design of a software system to be mathematically verified as complete and correct, even before a single line of code has been written.

The logo for Verum, consisting of the word "verum" in a lowercase, sans-serif font with a registered trademark symbol (®) to its upper right. The logo is white and is centered within a solid black rectangular background.

Tools for building
mathematically
verified software

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